ABSTRACT OF DISCLOSURE

There is provided a media access controller with a power-save mode. Particularly, the media access controller of the present invention minimizes power loss by disabling clocks applied to all blocks, including CPU, of the media access controller during the power-save mode. The media access controller of the present invention includes: a power-save master for securing stable transmission/reception of data through bus by respective processors contained in the controller; a wake-up timer for noticing that the power-save mode is expired; a power control unit for determining whether to supply a power to a phase-locked loop, and a timing when clocks for the media access controller are applied and disabled; and a locktime register for storing a locktime when an output of the phase-locked loop is settled. Additionally, there is provided a method of efficiently changing the media access controller from the active mode to the power-save mode, and vice versa.

J:\SAM\0533\0533patapp2.doc